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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,310	09/26/2003	Akira Ishikawa	740756-2654	5329

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EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H-A

Office Action Summary	Application No.	Applicant(s)	
	10/670,310	ISHIKAWA, AKIRA	
	Examiner	Art Unit	
	Lex Malsawma	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *June 07, 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-25* is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 7, 2005 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1, 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Borel** (6,297,093 B1) in view of Assaderaghi et al. (6,424,011 B1; hereinafter "**Assaderaghi**").

Regarding claims 1, 2 and 4:

Borel discloses (in Figs. 2A-2C and Col. 2, lines 30-62) a semiconductor device manufacturing method, comprising the steps of:

forming a semiconductor film 1;

forming a gate insulating film 3 on the semiconductor film;

forming a gate electrode 4 on the gate insulating film 3;

adding a first impurity 11 to the semiconductor film while using the gate electrode 4 as a mask (Col. 2, lines 34-36);

forming a conductive film 21 over the gate insulating film and the gate electrode;

forming a sidewall 23/24 to a side surface of the gate electrode in a condition of the gate insulating and the gate electrode being covered by the conductive film 21; and

adding a second impurity 29 (Fig. 2C) to the semiconductor film while using the gate electrode and the sidewall as masks.

Borel discloses the device/method is to be incorporated with CMOS structure manufacturing (Col. 1, lines 51-52), wherein channel lengths in CMOS technology were well below 2.0 um (e.g., approaching 0.13 um) at the time the current invention was made. Furthermore, the device would obviously incorporate a logic circuit because a functional, electrically-programmable memory device, comprising memory cells formed by Borel's process, would obviously incorporate logic devices such as address decoders (row, column or x, y).

Borel **lacks** forming the semiconductor film over an insulating surface; however, note that Borel discloses forming a memory cell on bulk semiconductor. Assaderaghi **teaches** it was well known in the art that silicon-on-insulator (SOI) devices have significant advantages over bulk-semiconductor-type devices, wherein the advantages include performance increases of 30% (note Col. 1, lines 53-56). Assaderaghi shows (in Figs. 2a-2c) that an active device, such as a memory cell, formed on an SOI substrate will comprise a semiconductor film ("SOI") formed over an insulating surface ("BOX"), followed by forming a gate insulating film (34 or 107). It would have been obvious to one of ordinary skill in the art to modify Borel by utilizing a SOI substrate because Assaderaghi teaches that the SOI substrate would provide significant

performance increase, and when a SOI substrate is incorporated into Borel's process, a semiconductor film will be provided over an insulating surface prior to forming the gate insulating film 3 (as shown by Assaderaghi).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Borel** (in view of **Assaderaghi**) as applied to claim 1 above, and further in view of **Murai** (5,473,184).

Regarding claim 3:

Borel (in view of Assaderaghi) **lacks** specifying whether or not the second impurity 29 (Fig. 2C) is added through the combined layers (the conductive film and the gate insulating film). Murai is **cited only to show** it was very well known in the art that an impurity 7 can be added through a combination of two layers 2, 5 (note Figs. 2-3). Since Borel (in view of Assaderaghi) does not provide specifics regarding the second impurity, it would have been obvious to one of ordinary skill in the art to modify Borel (in view of Assaderaghi) by specifically reciting that the second impurity is added through the combined layers because Murai shows it was well known in the art to do so.

5. Claims 5-8 rejected under 35 U.S.C. 103(a) as being unpatentable over **Borel** (6,297,093 B1) in view of **Assaderaghi** (6,424,011 B1) and **Murai** (5,473,184).

Regarding claims 5-8:

These claim are similar to claims 1-4 (addressed in detail above) except for the additional limitation for forming an insulating film over the gate insulating film and the gate electrode before forming the conductive film. Borel (in view of Assaderaghi) discloses all limitations

within these claims **except for** the additional limitation. Murai **teaches** (in Figs. 1-2 and Col. 3, lines 43-46) that an insulating layer 5 formed over a gate insulating film 2 and a gate electrode 3 provides an effective etching stopping film during later etching processes. It would have been obvious to one of ordinary skill in the art to modify Borel (in view of Assaderaghi) by forming and insulating layer as taught by Murai because the insulating layer would serve as an effective etch-stopping layer during later processing steps. *Specifically regarding claim 7*: This claim is similar to claim 3 (addressed in detail above), therefore, it is held obvious over the cited references for reasons similar to those applied to claim 3 above.

6. Claims 9, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Borel** (6,297,093 B1) in view of **Assaderaghi** (6,424,011 B1) and Papadas et al. (5,687,113; hereinafter "**Papadas**").

Regarding claims 9, 10 and 12:

These claim are similar to claims 1, 2 and 4 (addressed in detail above) except for the additional limitations of removing the sidewall and the conductive film. Borel discloses removing the conductive film 21 (note Fig. 2C); however, Borel (in view of Assaderaghi) **lacks** removing the sidewall. It is important to note that Borel incorporates Papadas by reference (see Borel, Col. 1, lines14-16 and Col. 2, lines 63-65). Papadas **teaches** (in Figs. 3C-3D and Col. 6, lines 49-52) sidewall removal before forming contacts is a matter of design choice, i.e., note Papadas specifies, "if desired, the spacer 29 near the source side is removed". Borel is essentially a modification of Papadas, wherein the modification lies in the addition of the conductive film 21 (note again, Borel, Figs. 2A-2B); and given Papadas' disclosure regarding

sidewall removal, it would have been obvious for one of ordinary skill in the art to modify Borel (in view of Assaderaghi) by removing the sidewall because Papadas specifies that such a removal is merely a matter of choice/preference.

7. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Borel** (in view of **Assaderaghi** and **Papadas**) as applied to claim 9 above, and further in view of **Murai** (5,473,184).

Regarding claim 11:

This claim is similar to claim 3 (addressed in detail above), accordingly, this claim is held obvious over the cited references with reasoning similar to that applied to claim 3 above.

8. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Borel** (6,297,093 B1) in view of **Assaderaghi** (6,424,011 B1), **Murai** (5,473,184) and **Papadas** (5,687,113).

Regarding claims 13-16:

These claims are similar to claims 5-12, i.e., independent claim 13 is essentially a combination of claims 5 and 9 (which were addressed in detail above). Borel (in view of Assaderaghi) discloses all limitations in claim 13 **except** form forming an insulating film (over the gate insulating film and the gate electrode) and removing the sidewall. As explained in detail above, Murai **teaches** that an insulating film, formed over a gate insulating film and a gate electrode, will serve as an effective etch-stopping layer; and Papadas **teaches/shows** that sidewall removal is a matter of design choice (see above, "*Regarding claims 5-8*" and

"*Regarding claims 9, 10 and 12*"). As explained above, it would have been obvious to one of ordinary skill in the art to modify Borel by incorporating an insulating layer (as taught by Murai) and by removing the sidewall (as taught by Papadas) because Murai teaches the insulating layer would provide an effective etch-stopping layer during later processing steps and Papadas teaches that sidewall remove is a merely a matter of choice/preference.

Allowable Subject Matter

9. Claims 17-25 are allowable over the references of record.

10. The following is a statement of reasons for the indication of allowable subject matter:

Claims 17-20 are allowable primarily because claim 17 recites a limitation for adding the second impurity through the conductive film and the gate insulating film while using the gate electrode and the sidewall as masks. In other words, this limitation in combination as recited in claim 17 requires a portion of the conductive film to remain underneath the sidewall during the second impurity-addition step, where such an arrangement also requires the conductive film to be in contact with the gate electrode. The combination of process steps cannot be fairly suggested by the references of record.

Claims 21-25 are allowable primarily because claim 21 requires forming a sidewall over the conductive film to a side surface of the gate electrode, i.e., this limitation in combination as recited in claim 21 cannot be fairly suggested by the references of record.

Remarks

11. Applicant's remarks/arguments presented in the response filed May 09, 2005 have been carefully reviewed and considered, and in reference to claims 1-16, the remarks/arguments are not persuasive for the following reasons.

With respect to claims 1, 2 , 4 and 13-16, the remarks/arguments are moot in view of the new grounds of rejection presented in this Office action. In response to the applicant's request for further explanation of how a logic circuit is disclosed by Borel, one explanation has been provided above, additionally, the examiner agrees with the applicant's statement that "a device with CMOS structure is widely used"; accordingly, one of ordinary skill in the art realizes that a CMOS structure provides at least a logic circuit because a CMOS structure comprises Complementary-Metal-Oxide-Semiconductor transistors, i.e., a CMOS structure comprises at least one p-channel transistor (PMOS) and one n-channel transistor (NMOS), and a circuit comprising PMOS and NMOS transistors would certainly be a logic circuit, since each transistor (PMOS or NMOS) is essentially a switch that can be turned on or off (i.e., logical "1" or "0").

With respect to claims 3 and 5, the applicant asserts that Murai does not disclose adding an impurity through a conductive film. However, both the gate oxide film and the silicon dioxide film (in Murai) at least "thermally" conductive, even if the two films may not be "electrically" conductive. Therefore, the applicant's remarks/arguments are not persuasive, especially because the claimed invention does not require the conductive film to be "electrically" conductive.

With respect to claims 9, 10 and 12, applicant's remarks/arguments are not persuasive because the material composition of the sidewall spacers is not relevant to either the claimed invention or to the reasoning provided for combining the applied references. In other words,

Papadas (which Borel incorporates by reference) is cited only to show that, during subsequent processing to complete Borel's device (i.e., processing beyond the process steps disclosed by Borel), removal of the sidewall spacers is purely a matter of choice for a practitioner who incorporates Borel's teachings; therefore, the material composition of Papadas' sidewall spacer is not relevant to the reasoning provided for combining the references.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon. - Thur. (4-12 hours between 5:30AM and 10 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

June 21, 2005